

1 1. **(Currently Amended)** An ATM slave interface unit providing an
2 interface between an ATM master processing unit and a direct
3 memory access unit coupled to an ATM slave processing unit, the
4 interface unit comprising:

5 an input unit, the input unit receiving data cells and
6 exchanging control signals with the ATM master processing unit;

7 an input buffer unit including:

8 a buffer storage unit; and

9 a calculation unit, wherein the input buffer unit
10 receives data signals from and exchanges control signals with the
11 input unit, the input buffer unit storing received data cells in
12 the buffer storage unit, the buffer storage unit transferring data
13 cells to the ~~ATM slave processing~~ direct memory access unit; and

14 a register, each data cell including a cell ~~location~~ portion
15 ~~identifying a~~ having an encoded destination location, the
16 calculation unit responsive to the contents of the register and to
17 the ~~data cell~~ portion for generating a destination location
18 ~~control signal~~ for the data cell in the ATM slave processing unit.

19
20 2. **(Currently Amended)** The interface unit as recited in
21 claim 1 wherein the buffer storage unit is a first-in/first-out
22 memory unit.

23
24 **Please amend Claim 3 as follows.**

25
26 3. **(Currently Amended)** The interface unit as recited in
27 claim ~~1~~ 2 wherein the first-in/first-out memory unit can store at
28 least two data cells.

29
30 4. **(Original)** The interface unit as recited in claim 1
31 wherein the buffer storage unit transfers a data cell to the slave
32 data processing unit every clock cycle.

1 Please amend Claim 5 as follows.

2
3 5. (Currently Amended) The interface unit as recited in
4 claim 1 wherein the destination locations can be selected from at
5 least one of the group consisting of a ~~plurality of central~~ slave
6 processing unit, a ~~plurality of~~ shared memory location for a
7 plurality of slave processing units, and at least one ~~central~~
8 slave processing unit and at least one shared memory location.

9
10 Please amend claim 6 as follows.

11
12 6. (Currently Amended) The interface unit as recited in
13 claim 1 further comprising:
14 an output buffer unit; the output buffer unit including a
15 buffer storage unit, the buffer unit storing data cells, the
16 output buffer unit receiving data cells from the ~~slave processing~~
17 direct memory access unit the data buffer unit exchanging control
18 signals with the slave processing direct memory access unit; and
19 an output unit; the output unit receiving data cells from the
20 output buffer unit and applying data cells to the ATM master
21 processing unit, the output unit exchanging control signals with
22 the output buffer unit and with the ATM master processing unit.

23
24 7. (Original) The interface unit as recited in claim 1
25 wherein the ATM slave processing unit includes at least one
26 digital signal central processing unit.

27
28 Please amend Claim 8 as follows.

29
30 8. (Currently Amended) The interface unit as recited in
31 claim 1 wherein the control signals and the data cells have ~~the~~ a
32 UTOPIA format.

1 Please cancel Claim 9.

2
3 9. (Currently Cancelled) The interface unit as recited
4 in claim 1 wherein the ATM slave processing unit includes a direct
5 memory access unit.
6

7 Please amend claim 10 as follows.
8

9 10. (Currently Amended) A method for exchanging data
10 cells from an ATM master processing unit with a plurality of
11 locations in an ATM slave processing unit, the ATM slave
12 processing unit including a direct memory access unit, the method
13 comprising:
14 storing data cells from the ATM master processing unit in a
15 buffer storage unit;
16 comparing a field in the data cell with the contents of a
17 register to determine the destination location of the data cell;
18 generating a signal identifying the destination location; and
19 when storage space is available, transferring a data cell
20 from the buffer storage unit to the ~~destination location~~ direct
21 memory access unit.
22

23 11. (Original) The method as recited in claim 10
24 further comprising:
25 implementing the buffer storage to hold two data cells; and
26 transferring a data cell from the buffer storage unit to the
27 ATM slave processing unit on consecutive clock cycles.
28

29 12. (Original) The method as recited in claim 11
30 further comprising implementing the control signals in a UTOPIA
31 format.
32

1 Please amend Claim 13 as follows.

2
3 13. (Currently Amended) The method as recited in claim 10
4 wherein ~~the ATM slave processing unit includes a direct memory~~
5 ~~access unit~~, the method ~~including~~ includes applying the signal
6 identifying the destination location to the direct memory access
7 unit.

8
9 Please amend Claim 14 as follows.

10
11 14. (Currently Amended) A data processing system
12 comprising:
13 an ATM master processing unit;
14 an ATM slave processing unit, the ATM slave processing unit
15 including a direct memory access unit; and
16 an ATM slave interface unit, the slave interface unit
17 including:
18 an input unit, the input unit receiving data signals
19 from the ATM master unit, the input unit exchanging control
20 signals with the ATM master unit;
21 an input buffer storage unit, the input buffer unit
22 including:
23 a memory unit; and
24 a calculation unit, wherein the input buffer unit
25 exchanges control signals with the input unit, the input buffer
26 unit storing data cells in the memory unit, the buffer storage
27 unit transferring data cells to the ATM slave processing unit, the
28 input buffer unit exchanging control signals with the ~~ATM slave~~
29 ~~processing unit~~ direct memory access unit; and
30 a register, the contents of the register identifying
31 ~~the~~ destination location field in a data cell, the contents of the
32 register providing the translation of field in the data cell ~~to~~
33 into a destination location, wherein the calculation unit

1 generates a destination location signal and applies the
2 destination location signal to the ATM slave processing unit.

3
4 **Please cancel Claim 15.**

5
6 15. **(Previously Cancelled)**

7
8 16. **(Original)** The data processing system as recited in
9 claim 14 wherein the memory unit is a first-in/first-out memory
10 unit capable of storing at least two data cells.

11
12 **Please amend Claim 17 as follows.**

13
14 17. The data processing system as recited in claim 16
15 wherein the input buffer unit transfers data cells to the ATM
16 slave processing unit on consecutive ~~lock~~ clock cycles.